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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,601	10/23/2001	Edward L. Hepler	I-2-183.1US	5329

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EXAMINER	
ABRISHAMKAR, KAVEH	
ART UNIT	**PAPER NUMBER**
2131	

DATE MAILED: 03/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/046,601	HEPLER, EDWARD L.	
	Examiner	Art Unit	
	Kaveh Abrishamkar	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,6 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 27, 2005 has been entered.

2. Claims 1-2, 4, 6, and 8 are currently being considered.

Response to Arguments

3. Applicant's arguments with respect to claims 1-2, 4, 6, and 8 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2,4,6, and 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Naruse (U.S. Patent 6,115,410) in view of Dabak et al. (U.S. Patent No. 6,798,737).

5. Naruse and Dabak are analogous art because both deal in generating Walsh cods for signal processing purposes.

6. With respect to claim 1, Naruse discloses a system for generating an OVSF code comprising:

A binary counter for providing a binary count comprising a plurality of sequential M-bit binary numbers (column 5 lines 51-56);

An index selector, for providing an M-bit binary identification of said OVSF code (column 5, lines 51-56); and

A logical reduction means having a first input from the counter and a second input from the index selector and having an output; whereby the desired OVSF code is output from said output (column 5 lines 59-67).

7. Naruse does not disclose a system comprising:

Bit reordering means, for selectively reordering the bits of each said binary number from least significant bit to most significant bit.

Dabak discloses a system comprising:

Bit reordering means, for selectively reordering the bits of each said binary number from least significant bit to most significant bit (column 4 lines 52-66), wherein for Walsh codes with lower spreading factors, the inputs which use the same Walsh code must be in bit-reversed order.

8. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Dabak with the teachings of Naruse for the Walsh codes with lower spreading factors to so that the codes can be used in the multi-rate versions (Dabak: column 4 lines 27-36).

9. With respect to claim 8, Naruse does not disclose a code generator further comprising a switch coupled to said bit reordering means, whereby when the switch is in a first position, the bit reordering means is coupled to the output of said counter to reorder the bits of said binary number, and when the switch is in a second position, the bit reordering means is decoupled from the output of said counter and the bits of said binary number are not reordered.

Dabak discloses a code generator further comprising a switch coupled to said bit reordering means, whereby when the switch is in a first position, the bit reordering means is coupled to the output of said counter to reorder the bits of said binary number, and when the switch is in a second position, the bit reordering means is decoupled from the output of said counter and the bits of said binary number are not reordered (column

4 lines 52-66), wherein for Walsh codes with lower spreading factors, the inputs which use the same Walsh code must be in bit-reversed order.

10. It would have been obvious to one of ordinary skill in the art at the time of invention to have combined the teachings of Dabak with the teachings of Naruse for the Walsh codes with lower spreading factors to so that the codes can be used in the multi-rate versions (Dabak: column 4 lines 27-36).

11. With respect to claim 2, Naruse discloses a code generator for generating individual binary codes of a set of binary codes, each binary codes having 2^M bits, the code generator comprising:

a counter having an output and sequentially outputting M-bit counts in a parallel orientation, each successive count being incremented by 1 (column 5, lines 51-56);

an index selector for outputting an M-bit code identifier in a parallel orientation (column 5 lines 51-56);

a parallel array of M logical gates, each having an output and a first input being one parallel bit from said bit ordering means and a second input being one parallel bit from said index selector (column 5, lines 59-67); and

and a reduction network of logical gates associated with the outputs of said parallel array of logical gates for outputting a single code bit each time a parallel M-bit count is input to said parallel logical gate array from said bit ordering means, such that

the binary code which is identified by the M-bit code identifier is produced after 2^M iterations (column 5 lines 59-67).

12. Naruse does not disclose a system comprising:

Bit reordering means, coupled to said output of said counter, for receiving each M-bit count, whereby the M-bit counts are ordered from least significant bit to most significant bit, and whereby said bit reordering means reorders the bits from most significant to least significant bit.

Dabak discloses a system comprising:

Bit reordering means, for selectively reordering the bits of each said binary number from least significant bit to most significant bit (column 4 lines 52-66), wherein for Walsh codes with lower spreading factors, the inputs which use the same Walsh code must be in bit-reversed order.

13. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Dabak with the teachings of Naruse for the Walsh codes with lower spreading factors to so that the codes can be used in the multi-rate versions (Dabak: column 4 lines 27-36).

14. With respect to claim 4, Naruse discloses a system for generating a desired pseudorandom code comprising:

a binary counter for providing a plurality of M-bit sequential binary numbers (column 5 lines 51-56);

an index selector, for outputting an M-bit code identifier of the desired pseudorandom code (column 5 lines 51-56);

at least M logical gates, each having a first input from the said bit ordering means and a second input from the index selector, and each having an output (column 5 lines 59-67);

and an XOR tree for XORing said outputs of said logical gates to provide an XORed output; whereby the desired pseudorandom code is output from said XORed output (Figure 4).

15. Naruse does not disclose a system comprising:

Bit reordering means for reordering the bits of said binary counter from least significant bit to most significant bit.

Dabak discloses a system comprising:

Bit reordering means for reordering the bits of said binary counter from least significant bit to most significant bit (column 4 lines 52-66), wherein for Walsh codes with lower spreading factors, the inputs which use the same Walsh code must be in bit-reversed order.

16. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Dabak with the teachings of Naruse for

the Walsh codes with lower spreading factors to so that the codes can be used in the multi-rate versions (Dabak: column 4 lines 27-36).

17. With respect to claim 6, Naruse discloses a code generator for generating an individual binary code from a set of N binary codes, each binary code having M bits, the code generator comprising:

a counter having an output and sequentially outputting M-bit binary numbers, each successive binary number being incremented by 1 (column 5 lines 51-56);

an index selector for outputting an M-bit code (column 5 lines 51-56);

a logical gate array having a first input from said bit ordering means and a second input from said index selector, and having an output (column 5 lines 59-67);

a reduction network of logical gates associated with the output of said logical gate array for outputting a single code bit each time an M-bit binary number is input to said logical gate array from said bit reordering means, such that the binary code identified by the M-bit code is produced after 2^M iterations (column 5 lines 59-67).

18. Naruse does not disclose a system comprising:

bit reordering means, coupled to said output of said counter, for receiving each M-bit binary number having bits ordered from least significant bit to most significant bit, whereby said bit reordering means reorders the bits from most significant bit to least significant bit.

Dabak discloses a system comprising:

bit reordering means, coupled to said output of said counter, for receiving each M-bit binary number having bits ordered from least significant bit to most significant bit, whereby said bit reordering means reorders the bits from most significant bit to least significant bit (column 4 lines 52-66), wherein for Walsh codes with lower spreading factors, the inputs which use the same Walsh code must be in bit-reversed order.

19. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Dabak with the teachings of Naruse for the Walsh codes with lower spreading factors to so that the codes can be used in the multi-rate versions (Dabak: column 4 lines 27-36).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaveh Abrishamkar whose telephone number is 571-272-3786. The examiner can normally be reached on Monday thru Friday 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KA
03/23/2006

CHRISTOPHER REVAK
PRIMARY EXAMINER

3/24/06